

REMARKS

Claims 1-17 were previously pending in this application. Claims 11-17 stand withdrawn as non-elected and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 1-4 and 6-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Pat. No. 6,373,119 issued to Noda (“Noda”) and U.S. Pat. NO. 6,294,823 issued to Arafa et al. (“Arafa”).

Claim 5 stands rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Noda and Arafa, as applied to claims 1-4 and 6-10, and further in view of U.S. Pat. No. 6,319,794 issued to Akatsu et al (“Akatsu”).

Claims 1-10 remain in the case for reconsideration.

Reconsideration is respectfully requested.

Claim Rejections – 35 USC § 103

Claims 1-4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Noda and Arafa.

Claim 5 stands rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Noda and Arafa, as applied to claims 1-4 and 6-10, and further in view of Akatsu.

The rejection of claims 1-10 under 35 U.S.C. 103 (a) is respectfully traversed.

The Examiner states in the office action that “Noda discloses a semiconductor substrate (1); a device isolation region (20) ...the device isolation region having a *protrusion* that is higher than that the top surface of the semiconductor substrate.” (“Emphasis added”)

However, the protrusion of the device isolation region 20 of Noda needs to be planarized, i.e. removed. See FIG. 6B and col. 3, lines 50-53 and col. 7, lines 30-35. What is more, at col. 8, lines 4-11, Noda states that:

“[S]ince the cap insulation layer 5 can be embedded in the element separation trench as shown in FIG. 3, the surface under the gate electrode can be made flat. Accordingly, in the photolithograph process to be conducted for patterning of the gate electrode, it becomes possible to control the influence of such as the change of resist thickness or halation to the minimum and perform the further delicate processing.”

Thus, if the protrusion is not removed, it would not form the device intended by Noda. Therefore, Noda teaches away from the claimed invention.

For these reasons, Noda does not teach, as recited in claim 1,:

“the device isolation region having *a protrusion* that is higher in level than the top surface of the semiconductor substrate;

...

an etch stop *spacer* formed *overlying a sidewall of the protrusion*.”

(“Emphasis added”)

Also, even if Noda is combined with Arafa, it would not teach or suggest the features included in claim 1 because the combination would merely teach an etch stop spacer formed below the top surface of the substrate, not an etch stop *spacer* formed *overlying a sidewall of the protrusion*.

Thus, applicant respectfully submits that the Examiner has not presented a *prima facie* case of obviousness. Accordingly, the rejection of claim 1 should be withdrawn. Also, claims 2-10, which depend from claim 1, recite additional features that are not disclosed or suggested by the prior art, and are therefore allowable, based on this dependency, and based on the dependent claims themselves.

For the foregoing reasons, reconsideration and allowance of claims 1-10 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

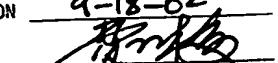
Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Cancel claims 11-17, without prejudice.